BeiJing University of

Post and Telecomunication

Student NO.:2013213201

Class NO.:2013215109

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Dr.Zheng Feng

**LABORATORY REPORY**

**DIGITAL CIRCUIT DESIGN**

**INTRODUCTION TO DESIGN USING VHDL**

**INTRODUCTORY SUMMARY**

Last week you sent us an E-mail to tell us the details about our third Lab. on Thursday. Meanwhile we had been given a sheet which can lead us to complete this laboratory and then we should fill the blanks. The aims of this Lab Session are to learn how to use VHDL and ModelSim to design and simulate some basic logic circuits,namely:a NAND gate and three types of Adders.

**LAB MATERIALS(VHDL)**

Our lab analysis relies on the results of the code which you complete in the computer and compile successfully. So you should just have a computer with the programming software**.**

**LAB PROCEDURE**

Once we receive a code requirement, we should create a 'New Project' and then we should follow:

a:Open the Xilinx Project Navigator tool.

b:Create a directory where you wish to save your project as indicated by the example.

c: After filling in the appropriate fields(as suggested),click the Next>button.

Here is some information about the options:

a:Device Family: We will be using an FPGA device of the Spartan2 device family, which has densities of up to 200000

b:The Spartan2 device family has six different devices. In our case, we can use the smallest device in this family, as it provides 15000 gates!

c:Package: This refers to the type and number of pins for the chosen chip.

**CONCLUSION**

The entire lab makes ourselves master of the knowledge about the NADA Gate. And we should forecast the results first and then compare the results in the laboratory to test the final results. This laboratory require us to connect knowledge about the digital circuit and apply them in the lab. But I still have some problems can't be resolve by ourselves, so I suggest you can give us a lesson to explain these questions.

I will call you this weekend to discuss our study and any possible following-up you may wish us to do.

Sincerely,

Pang Yuanyuan